ABSTRACT

Error correction on high speed interconnection links - backplane or extended wires (cable, optical fiber) - is exhaustively considered by many telecommunication vendors, especially those who offer "scalable router' products. Since the 64b/66b encoding scheme is a strong candidate of high speed interconnection protocol, error correction on 64b/66b encoded links is of interest. Although the IEEE 802.3 10G Ethernet standard does not specifically refer to packet loss, it can be shown that even only a single-bit error correction can significantly enhance the quality of the link. The present invention presents a simple and fast error-correction scheme that can be used in conjunction with the 64b/66b encoding in products where intra-board (chip-to-chip) or inter-shelf interconnections of high speed elements are required. It utilizes the CRC16 to optimize on error detection, correction, or both: it detects and corrects all single-bit errors and detects all multiple-bit errors.